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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/809,164
Filing Date: March 25, 2004
Appellant(s): SCHULTZ, ROBERT J.

Mark Wilson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/6/2009 appealing from the Office action mailed 6/1/2009

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6272621	Key	8-2001
20030041163	Rhoades	2-2003

7193997	Van Luteren	3-2007
200300121198	Kaganoi	1-2003
7219187	Khanna	5-2007

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163).

Regarding claim 12, Key teaches an array of processing elements **(Fig. 3 PEs)** having; at least one first stage processing element **(Fig. 3 the first PE 400)**; and at least one second stage processing element **(Fig. 3 the second row PE 400)**; and a first stage memory unit **(Fig. 3 the first 330)** that is searched in response to search information from the first stage processing element. However, Key does not expressly teach the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet. **Rhoades** teaches in **Fig. 8, Perform Table Lookup** is

processed in parallel with **Transmission Error Detection – Packet Lifetime Calculations**. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet in order to provide the optimal balance between the conflicting demands of speed and programmability (Paragraph 16, Rhoades).

3. Claims 1, 2, and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhoades et al. (US 20030041163) in view of Van Lunteren et al. (US Patent 7193997).

Regarding claim 1, Rhoades teaches performing a first search **(Fig. 8, Perform Table Lookup)** using a first stage processing element **(Fig. 8, Packet processing block, Determine Protocol-Initiate Lookup)** related to a packet using first search information **(Fig. 8, Extract Lookup Key)**; performing, in parallel with the first search, search-independent processing using a second stage processing element **(Fig. 8, Packet processing block, Transmission Error Detection–Packet Lifetime Calculations)** on information related to the packet **(Fig. 8, Perform Table Lookup** is processed in parallel with **Transmission Error Detection–Packet Lifetime Calculations)**; and performing search-dependent processing using a result from the first search and a result of the search-independent processing **(Fig. 8, Process Lookup**

Result-Complete Tunneling Task). However, Rhoades does not teach producing second search information. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce search information. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to produce second search information in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 2, Rhoades and Van Lunteren teach the limitations for claim 1 as applied above. Van Lunteren teaches in Fig. 10 performing a second search using the second search information.

Regarding claim 3, Rhoades and Van Lunteren teach the limitations for claim 2 as applied above. Rhoades teaches in Fig. 8 the processors synchronize with other processors and hardware accelerators via semaphores (holding a processing state from the search-independent processing until the result from the first search is available).

4. Claims 6, 7, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163) and Van Lunteren et al. (US Patent 7193997).

Regarding claim 6, Key teaches processing information related to a packet using a first stage processing element **(Fig. 3, the first PE 400)** to produce a first search key, wherein the first stage processing element is included within an array of processing elements; searching a first stage memory unit **(Fig. 3, the first 330)** using the first search key. However, Key does not teach performing, in parallel with the search of the

first stage memory unit, search-independent processing on information related to the packet using a second stage processing element, wherein the second stage processing element is included within the array of processing elements; performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and searching a second stage memory unit using the second search key. Rhoades teaches the limitations as applied to claim 12 above.

However, Key and Rhoades do not teach to produce a second search key; and searching a second stage memory unit using the second search key. Van Lunteren teaches as applied to claim 1 above. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to produce second search information in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 7, Key, Rhoades, and Van Lunteren teach the limitations for claim 6 as applied above. Key teaches the limitations as applied to claim 3.

Regarding claim 11, Key, Rhoades, and Van Lunteren teach the limitations for claim 6 as applied above. Key teaches in Fig. 8 row synchronization logic 800 ensuring that each PE stage completes its processing of current context prior to loading new context at a new phase (forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced).

Regarding claim 14, Key and Rhoades teach the limitations for claim 12 as applied above. However, Key does not expressly teach the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce a search key. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key in order to determine a plurality of predefined processing rules applies to a data packet (Col. 3 Lines 53-55, Van Lunteren).

Regarding claim 15, Key, Rhoades, Van Lunteren teach the limitations for claim 14. Van Lunteren teaches in Fig. 10 a second stage memory unit that is associated with the second stage processing element, wherein the search key is used to search the second stage memory unit.

5. Claims 13, 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Rhoades et al. (US 20030041163) and Kaganoi et al. (US PGPUB 20030012198).

Regarding 18, Key teaches an array of processing elements **(Fig. 3 a programmable arrayed processing engine, 400)** having; a plurality of first stage processing elements **(Fig. 3, the first row of PEs)**; and a plurality of second stage

processing elements **(Fig. 3, the second row of PEs)**; and a memory interface **(Fig. 3, 310)** that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements. However, Key does not teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets. Rhoades teaches the limitations as applied to claim 12 above. However, Key and Rhoades do not teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Regarding claims 13, Key and Rhoades teach the limitations for claim 12 as applied above. However, Key and Rhoades do not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention

was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Regarding claim 17, Key and Rhoades teach the limitations for claim 12. Kaganoi teaches in Fig.3 first stage memory unit comprises content addressable memory.

Regarding claim 20, Key, Rhoades, and Kaganoi teach the limitations for claim 18 as applied above. Key teaches in Fig. 8 row synchronization logic 800 ensuring that each PE stage completes its processing of current context prior to loading new context at a new phase.

Regarding claim 21, Key, Rhoades, and Kaganoi teach the limitations for claim 18 as applied above. Key teaches in Fig. 3 330 - memory bus.

6. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhoades et al. modified by Van Lunteren et al. as applied to claim 2 above, and further in view of Khanna (US Patent 7219187).

Regarding claim 4, Rhoades and Van Lunteren teach the limitations for claim 2 as applied above. However, Rhoades and Van Lunteren do not teach producing a comparand and a mask as the second search information. Khanna teaches in Col. 2 Lines 10-19 the CAM device can be instructed by the processor to compare a search key, also referred to as a comparand (e.g., generated from packet header data), with data stored in its associative memory array. Khanna further teaches in Col. 9 Lines 31-62 global mask select circuit 607 selects the corresponding global mask ID (GMID 622)

from search parameter table 525 in response to the activated GMSEL signal. The selected GMID is used to select a corresponding global mask GM(1) GM(z) from the global mask register 606 that globally masks the comparand data during a compare operation. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

Regarding claim 5, Rhoades, Van Lunteren, and Khanna teach the limitations for claim 4. Khanna teaches in Fig. 6 and Col. 9 Lines 31-62 Block select circuit 605 outputs block select signal BSEL 609 that enables comparand drivers 608 to drive the comparand data into CAM block array 602 to participate in a compare operation if a stored CAM table ID for the CAM array 602 matches one of the CAM table IDs provided from the search parameter table 525. The comparand data is globally masked by the selected global mask data by logically ANDing together the selected global mask data on a bit-for-bit basis with corresponding bits of the comparand data in the comparand drivers 608.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. modified by Rhoades and Van Lunteren et al. as applied to claim 6 above, and further in view of Khanna (US Patent 7219187).

Regarding claim 10, Key, Rhoades , and Van Lunteren teach the limitations for claim 6 as applied above. Khanna teaches the limitations as applied to claim 4 above. It

would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. modified by Rhoades and Van Lunteren et al. as applied to claims 6 and 7 above, and further in view of Kaganoi et al. (US PGPUB 20030012198).

Regarding claims 8 and 9, Key, Rhoades, and Van Lunteren teach the limitations for claims 6 and 7 as applied above. However, Key, Rhoades, and Van Lunteren do not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste at all times (Paragraph 50, Kaganoi).

Allowable Subject Matter

9. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

A. Claim 12

The Appellants argued:

(1) the Examiner does not provide articulated reasoning with some rational underpinning to address the "same packet" language of the claim. Specifically, there is no explanation or analysis in the Office Action to attempt to show how the Fig. 8 of Rhoades, Perform Table Lookup and the Transmission Error Detection - Packet Lifetime Calculations might operate with respect to the same packet.

(2) The combination of Key and Rhoades does not teach a second stage processing element that performs search-independent processing in parallel to the first stage processing unit. Although the Examiner asserts that Rhoades purportedly teaches this limitation, the Examiner's assertions fail to recognize that a table lookup is not search-independent processing as recited in the claim. While Fig. 8 of Rhoades shows a table lookup being performed in parallel with other operations, Rhoades does not teach that the table lookup is a search-independent operation. Rhoades cannot teach that the table lookup is a search-independent operation because a table lookup is in fact a search operation.

In response to Appellants argument, the examiner respectfully disagrees with the argument above.

In response to Appellants argument in sub-section (1), Fig. 8 of Rhoades is self-explanatory for one of ordinary skill in the art that *Perform Table Lookup* is performed in parallel with *Transmission Error Detection-Packet Lifetime Calculations*

respect to the same packet. It would be meaningless for *Transmission Error Detection-Packet Lifetime Calculations* and *Perform Table Lookup* to merge into *Process Lookup Result* for a packet if the *Lookup Result* is for a different packet.

In response to Appellants argument in sub-section (2), it is noted that the features upon which Appellant relies (i.e., a second stage processing element that performs search-independent processing in parallel to the **first stage processing unit**) are **not recited in the rejected claim**(s).

Appellant admits, as shown in sub-section (2) above and page 11 of Appeal Brief Under 37 D.F.R. § 41.37(a), "While Fig. 8 of Rhoades shows a table lookup being performed in parallel with other operations ... and a table lookup is in fact a search operation".

On page 9 of Appeal Brief Under 37 D.F.R. § 41.37(a), the examiner statement is listed from the Office Action, 3/9/09: "Rhoades teaches in Fig. 8, Perform Table Lookup (a search of a first stage memory unit) is processed in parallel with *Transmission Error Detection - Packet Lifetime Calculations* (a second stage processing element, to allow *a second stage processing element to perform search-independent processing* related to a packet in parallel with a search of the first stage memory unit)".

In view of the above, it is clear that Fig. 8 of Rhoades teaches the limitation of claim 12, "...configured to allow the second stage processing element **(Transmission Error Detection - Packet Lifetime Calculations)** to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit **(Perform Table Lookup)**, where the search is related to the same packet".

B. Claims 1, 2, and 3

The Appellants argued that "...the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of claim 1. Accordingly, Appellant respectfully asserts independent claim 1 is patentable over the combination of Rhoades and Van Lunteren because the combination of references does not teach the indicated limitations"

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claims 1, 2 and 3 are still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

C. Claims 6, 7, 11, 14, and 15

The Appellants argued that "...independent claim 6 is also patentable over the combination of Key, Rhoades, and Van Lunteren for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12"

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claims 6, 7, 11, 14, and 15 are still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

D. Claims 13, 17, 18, 20, and 21

The Appellants argued that "...independent claim 18 is also patentable over the combination of Key, Rhoades, and Kaganoi for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12".

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claims 13, 17, 18, 20, and 21 are still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

E. Claims 4 and 5

The Appellants argued that "...dependent claims 4 and 5 are also patentable over the cited references based on an allowable base claim".

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claims 4 and 5 are still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

F. Claim 10

The Appellants argued that "...dependent claim 10 is also patentable over the cited references based on an allowable base claim".

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claim 10 is still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

G. Claims 8 and 9

The Appellants argued that "...dependent claims 8 and 9 are also patentable over the cited references based on an allowable base claim".

In response to Appellants argument, the examiner respectfully disagrees with the argument above since claim 12 clearly disclosed by the combined system as set forth above. Thus, claims 8 and 9 are still not patentable for the same reason as set forth in claim 12. Please see the response set forth above in claim 12.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Eunsook Choi/

Examiner, Art Unit 2467

Conferees:

/Hong Cho/

Primary Examiner, Art Unit 2467

/Pankaj Kumar/

Supervisory Patent Examiner, Art Unit 2467